Hytera™

SERVICE MANUAL

DMR PORTABLE RADIO

DMR

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Revision History

Version	Date of Issue	Description
V00	2010-09	Initial Release

Copyright Information

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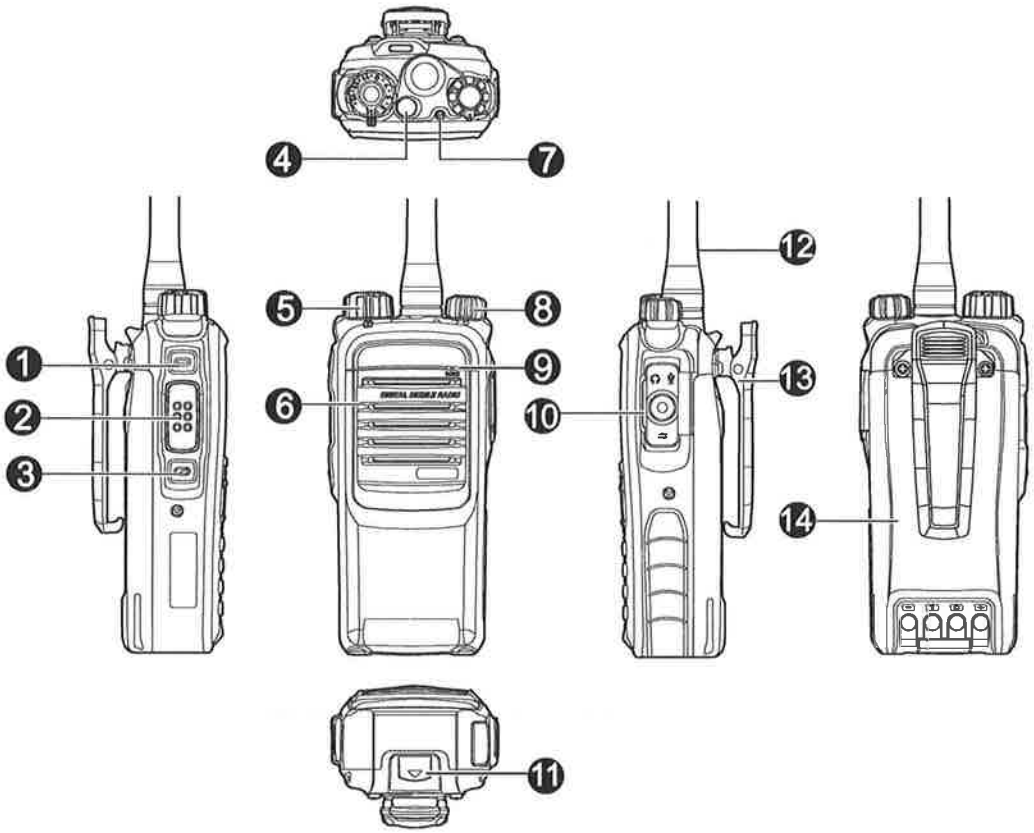
Introduction

Intended User

This manual is intended for use by qualified technicians only.

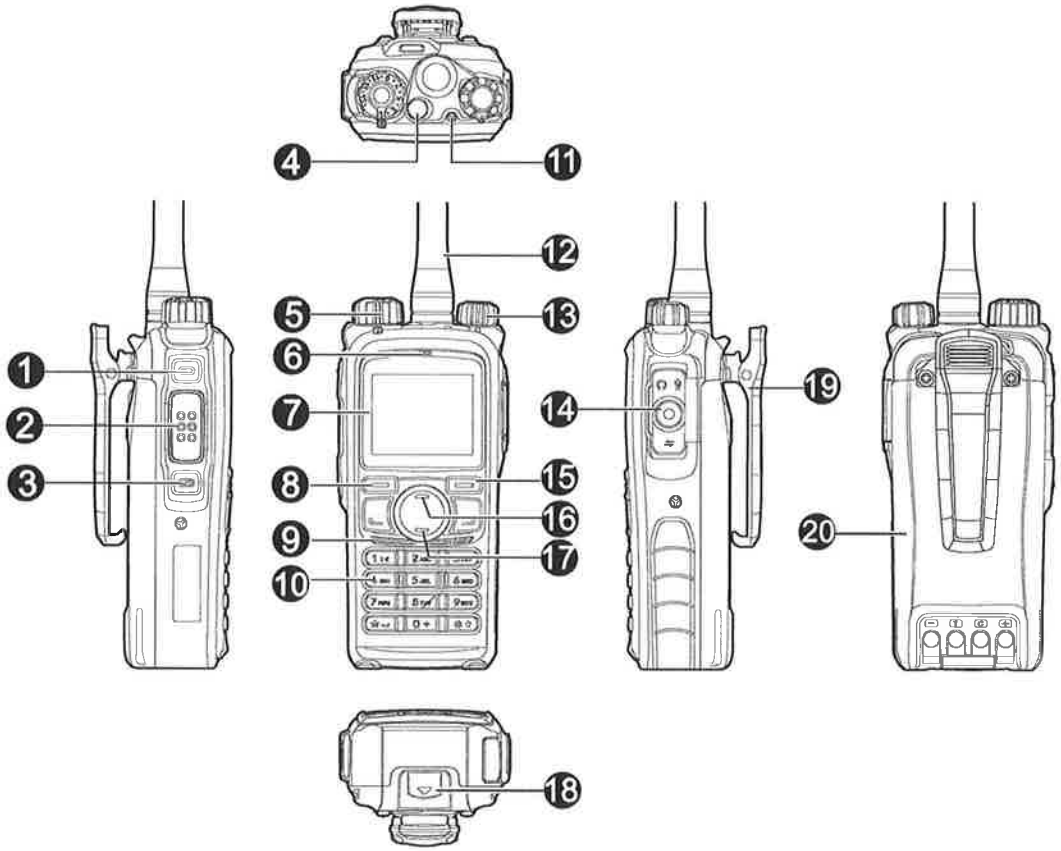
Product Controls

PD70X/ PD70XG/ HD705/ HD705G



No.	Part Name	No.	Part Name
①	SK1 (Side Key 1)	⑧	Radio On-Off/Volume Control Knob
②	PTT Key	⑨	Microphone
③	SK2 (Side Key 2)	⑩	Accessory Jack
④	TK (Top Key)	⑪	Battery Latch
⑤	Channel Selector Knob	⑫	Antenna
⑥	Speaker	⑬	Belt Clip
⑦	LED Indicator	⑭	Battery

PD78X/ PD78XG/ HD785/ HD785G



No.	Part Name	No.	Part Name
①	SK1 (Side Key 1)	⑪	LED Indicator
②	PTT Key	⑫	Antenna
③	SK2 (Side Key 2)	⑬	Radio On-Off/Volume Control Knob
④	TK (Top Key)	⑭	Accessory Jack
⑤	Channel Selector Knob	⑮	Back Key
⑥	Microphone	⑯	Up Key
⑦	LCD Display	⑰	Down Key
⑧	OK/Menu Key	⑱	Battery Latch
⑨	Speaker	⑲	Belt Clip
⑩	Numeric Keypad	⑳	Battery

Circuit Description

Note: The description related to the LCD is applicable to PD78X/ PD78XG/ HD785/ HD785G only, while the description related to GPS is applicable to PD70XG/ PD78XG/ HD705G/ HD785G only.

1. RF Section

1.1 TX Circuit

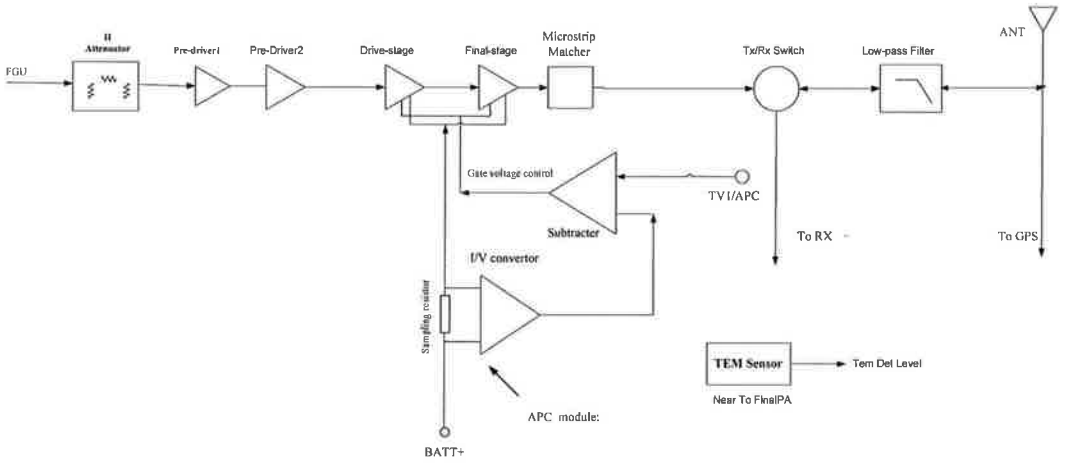


Figure 1 Diagram of TX Circuit

The TX circuit is mainly composed of:

① RF power amplifier circuit

② Low-pass filter circuit (for suppressing harmonics)

③ Auto power control circuit (APC) (including temperature detection circuit)

The carrier signal generated by TX VCO is modulated and amplified, and then feeds to the TX circuit. In this circuit, the signal passes through a II-type attenuator first, allowing certain isolation between the RF power amplifier circuit and TX VCO. Then it goes to a pre-driver amplifier (2SC3356) for pre-amplification, also providing certain isolation. After that, the signal goes to another pre-driver amplifier (2SC4988) and a driver amplifier (RD01) for further power amplification, to provide appropriate signal to the final-stage amplifier (RD07) for final power amplification. After processed by multiple amplifiers, the signal is processed by a microstrip matcher to complete output impedance matching, so as to reduce output power loss due to impedance mismatch. Then the signal passes through the TX/RX switch and goes to the low-pass filter.

The low-pass filter is a high-order Chebyshev filter composed of lumped-parameter inductors and capacitors. Via this filter, the spurious signal within the stop band can be attenuated as much as possible

while the in-band ripple is within the required range.

In the auto power control and temperature detection circuit, the drain current from the driver amplifier and final-stage amplifier is converted to voltage via the sampling resistor and subtraction circuit (composed of the first operational amplifier). This voltage is compared with the APC control voltage (output by DAC) at the second operational amplifier. Then the error voltage, which is output by the second operational amplifier, controls TX power by controlling the bias voltage at the gates of the amplifiers (including the driver amplifier and the final-stage amplifier). The temperature sensor detects the surface temperature of the final-stage amplifier, and converts it to DC voltage. Then the DC voltage is compared with the voltage corresponding to the protection temperature (generally 90% of the extreme temperature) of the amplifier. If the surface temperature is too high, the bias voltage of the amplifier will be reduced, so as to reduce output power. The bias voltage will not be increased until the surface temperature restores to normal level. This process will be repeated while the radio operates.

1.2 RX Circuit

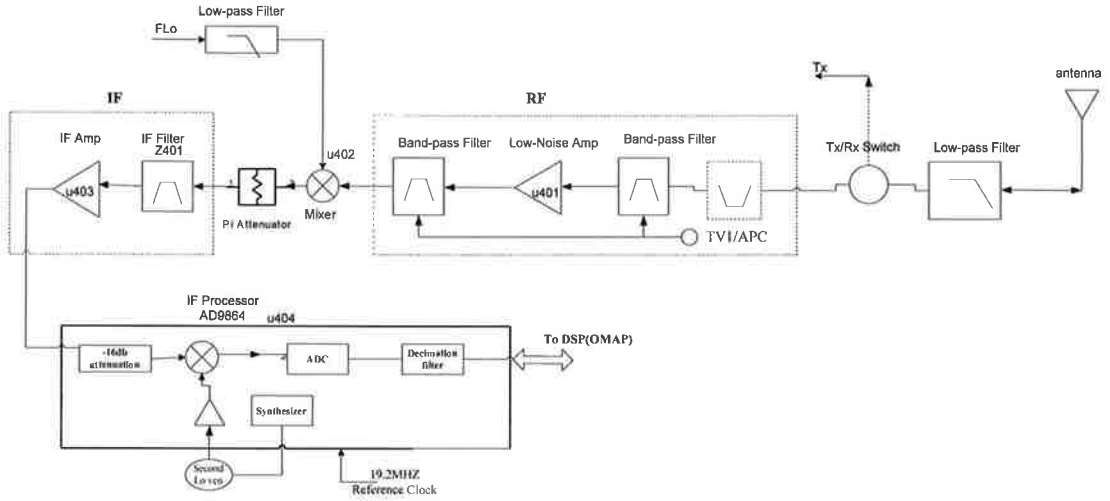


Figure 2 Diagram of RX Circuit

The RX circuit mainly comprises the RF band-pass filter, low-noise amplifier, mixer, IF filter, IF amplifier and IF processor.

1) Front-end Circuit

The HF signal from the low-pass filter passes through the electrically tunable band-pass filter controlled via APC/TV1 level, to remove out-of-band interference signal and to send wanted band-pass signal to the low-noise amplifier (Q9001). The amplified signal goes to a band-pass filter controlled via APC/TV1

level, to remove out-of-band interference signal generated during amplification, and to send wanted HF signal to the mixer.

The wanted signal passes through the RF band-pass filter and low-noise amplifier and goes to the mixer (D9017). Meanwhile, the first local oscillator (LO) signal generated by VCO passes through the low-pass filter and also goes to the mixer (D9017). In the mixer, the wanted signal and the first LO signal are mixed to generate the first IF signal (73.35MHz). Then the signal passes through a II-type attenuator (2dB) and the LC, to suppress carrier other than the first IF signal, and to increase the isolation between the mixer and the IF filter. After that, the first IF signal is processed by the crystal filter (Z9001), and is sent to the two-stage IF amplifier circuit (composed of 2SC3356) for amplification. Then the amplified signal goes to the IF processor AD9864(U401) for processing.

2) Rear-end Circuit

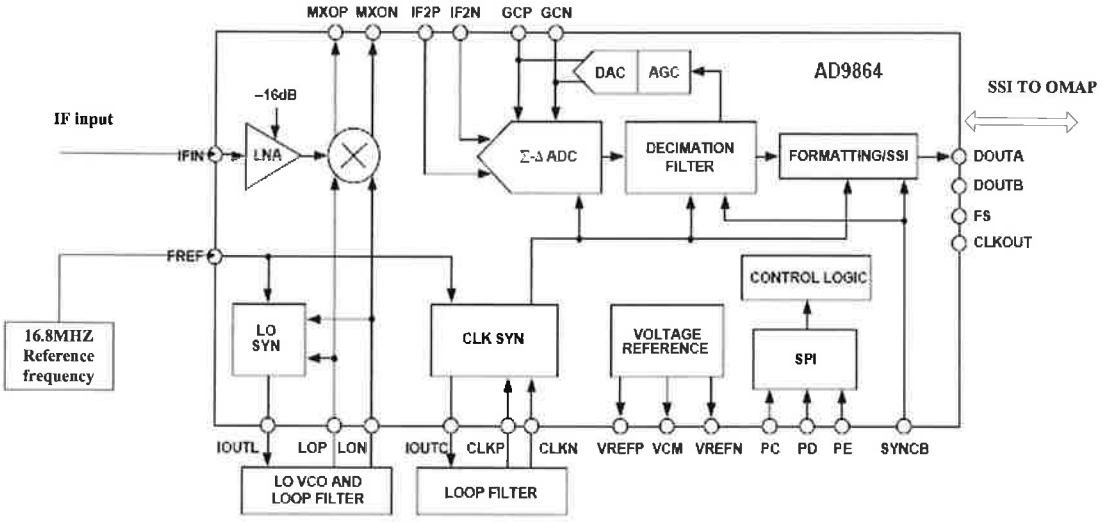


Figure 3 Diagram of IF Processor

The first IF signal (73.35MHz) output by the IF amplifier goes into AD9864 (U401) via Pin 47, where the signal is converted to the second IF signal (2.25MHz). Then the signal is converted to digital signal via ADC sampling, and output via the SSI interface. Finally, the digital signal is sent to DSP (OMAP5912) for demodulation.

AD9864 employs reference frequency of 19.2MHz and shares the crystal with OMAP. The second LO VCO comprises an oscillator, a varactor and some other components, to provide the 71.1/75.6MHz LO signal. The 18MHz clock frequency is generated by the LC resonance loop.

1.3 Frequency Generation Unit (FGU)

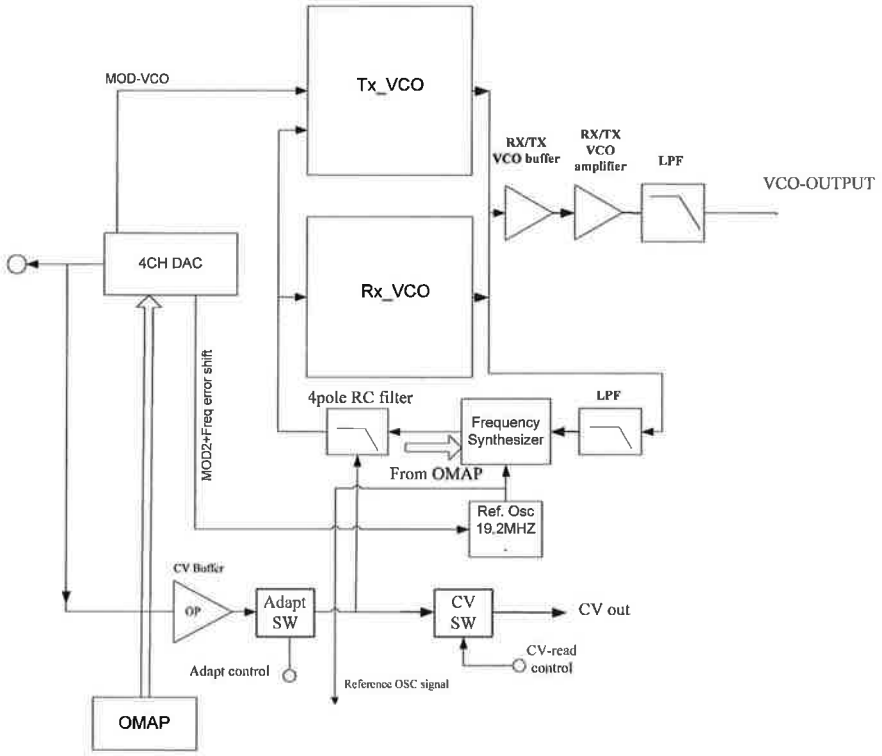


Figure 4 Diagram of FGU

The FGU is composed of VCO and PLL. It is the core module of the whole TX-RX system. This circuit provides accurate carrier frequency during transmission, and stable LO signal during reception. It has a direct influence on the performance of the system.

1) Working Principle of PLL

The 19.2MHz frequency generated by the reference crystal oscillator goes to PLL for division, generating the reference frequency (i.e. step frequency f1). Meanwhile, the frequency generated by VCO generates another frequency (f2) through the frequency divider in PLL. Then frequencies f1 and f2 are compared in the phase detector (PD), to generate continuous pulse current. The current goes to the loop filter for RC integration, and is then converted to CV voltage. Then the CV voltage is sent to the varactor of VCO. It adjusts the output frequency of VCO directly until the CV voltage becomes constant. Then PLL is locked, and the stable frequency output by VCO goes to the TX-RX channel after passing through two buffer amplifiers.

2) Working Principle of VCO

VCO employs Colpitts oscillator circuit (the RX oscillator circuit is composed of D102, D103, D106, D107 and L112; the TX oscillator circuit is composed of D108, D109, D110, D101 and L117). It obtains different output frequencies by changing the varactor's control voltage (i.e. CV voltage).

There are two types of VCO: TX VCO and RX VCO. Both types control EMD22 to switch operating status via OMAP. RX VCO is composed of the oscillator loop and Q104, to provide LO signal. TX VCO is composed of the oscillator loop and Q108, to provide carrier for TX signal.

3) Two-point Modulation

In TX mode, the two-point modulation technology is employed, to obtain higher modulation accuracy and lower 4FSK bit error rate. MOD-VCO and MOD-XO send the modulation signal to the modulation end of VCO and the reference crystal oscillator of PLL respectively to modulate TX VCO and the reference crystal oscillator.

1.4 GPS Circuit

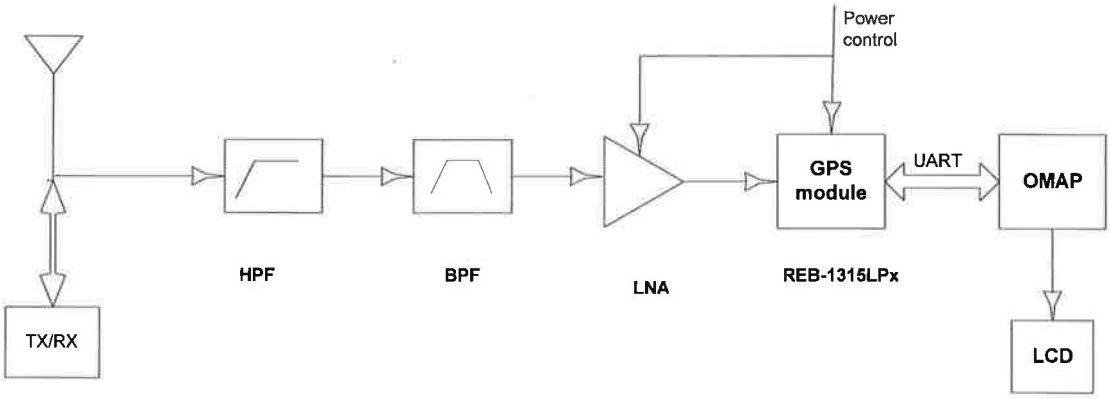


Figure 5 Diagram of GPS Circuit

The GPS function is realized via REB-1315LPx. The GPS circuit integrates a baseband processor, a LNA and a SAW. The 1575.42MHz GPS signal is received by the antenna, and then goes to HPF to remove the in-band signals used for transmission and reception. After that, the signal goes to BPF to further remove in-band signals, as well as harmonic and spurious signals. Then the weak GPS signal goes to a low-noise amplifier (LNA) for amplification. After amplified, the signal goes to the GPS module for further amplification and filtering, and is then sent to the baseband section for calculation. Then the calculated GPS positioning information is sent to OMAP via the UART interface. Meanwhile, OMPA can send appropriate command information to the GPS module via the UART interface. Finally, OMAP sends the processed data information to LCD.

2. Baseband Section

2.1 Power Section

2.1.1 Diagram of Power Control

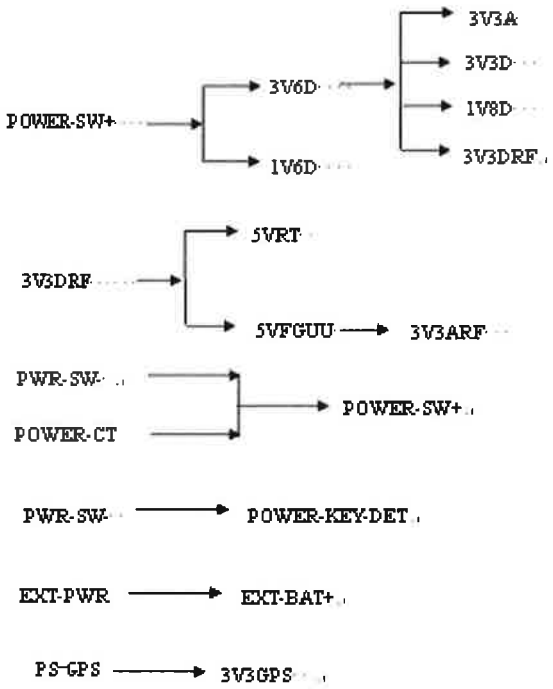


Figure 6 Diagram of Power Control

2.1.2 Radio On/Off

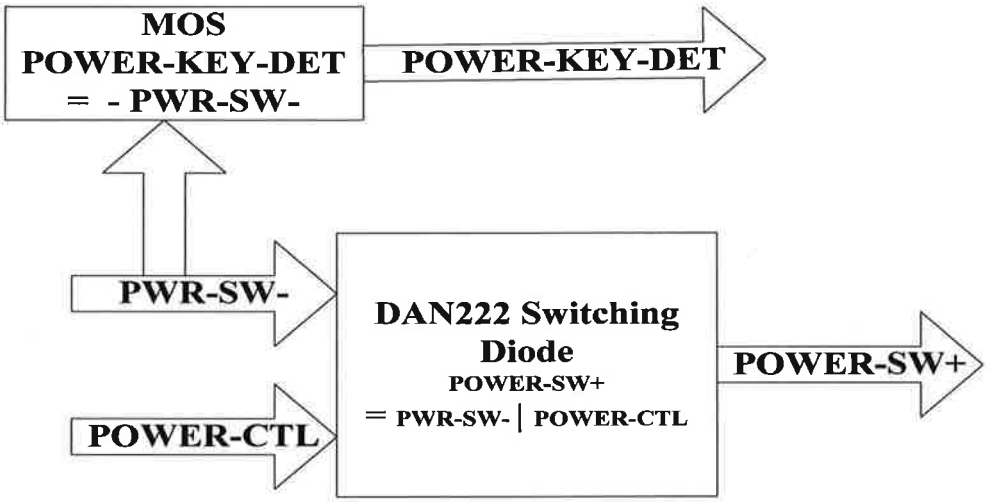


Figure 7 Diagram of Radio On/Off Control

The radio-on signal (POWER-SW+) satisfies the equation: POWER-SW+= PWR-SW- | POWER-CTL. When the Volume Switch is on, PWR-SW- and POWER-SW+ are at high level, and the radio powers up. After power-on, POWER-CTL goes to high level, and POWER-KEY-DET goes to low level. During power-off, POWER-SW+ is at low level, while POWER-KEY-DET is at high level. The system detects power-off procedure via POWER-KEY-DET and implements the power-off procedure. Then POWER-KEY-DET and POWER-SW+ go to low level, and the power is cut off.

2.1.3 Power Protection

Power protection includes over-current, reverse-voltage and ESD protection.

2.1.4 Power Consumption Control

OMAP can control and configure the power supply and working mode of the peripheral modules (RF section and baseband section) via I/O port and serial bus, so as to reduce power consumption.

2.2 Control Section

2.2.1 OMAP5912 Dual-core Processor

The radio uses the dual-core processor OMAP5912, which is mainly composed of ARM926EJ-S and TMS320C55xx. ARM926EJ-S is the main controller, while TMS320C55xx is used for modulation/demodulation and voice encoding/decoding.

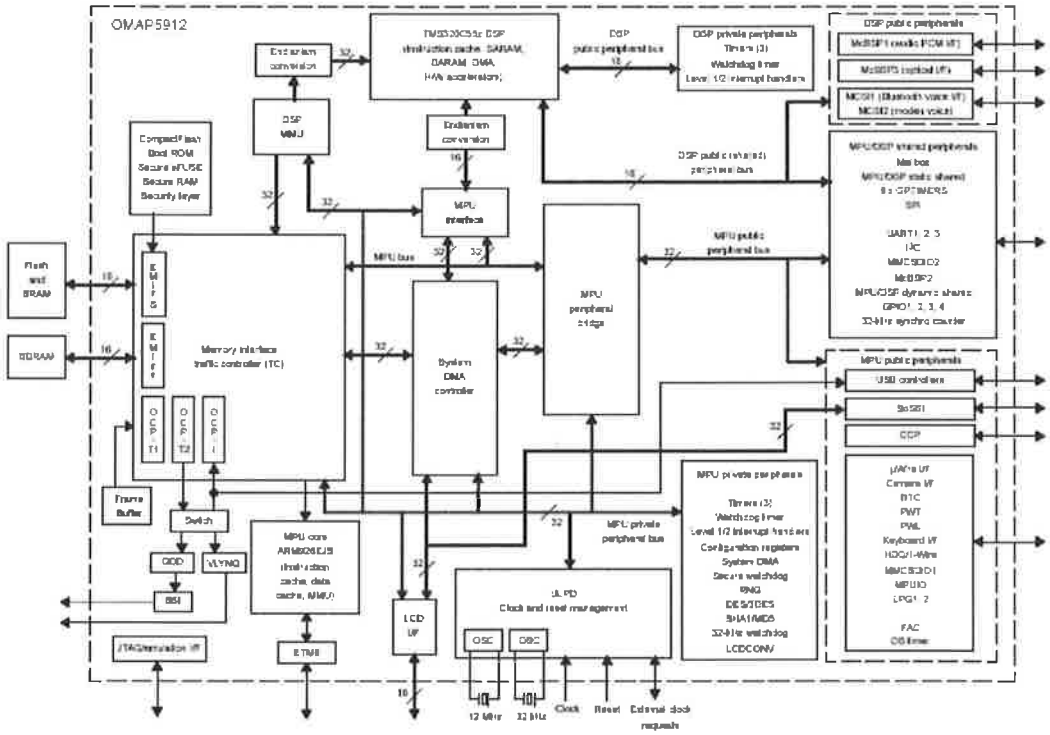


Figure 8 Diagram of OMAP5912

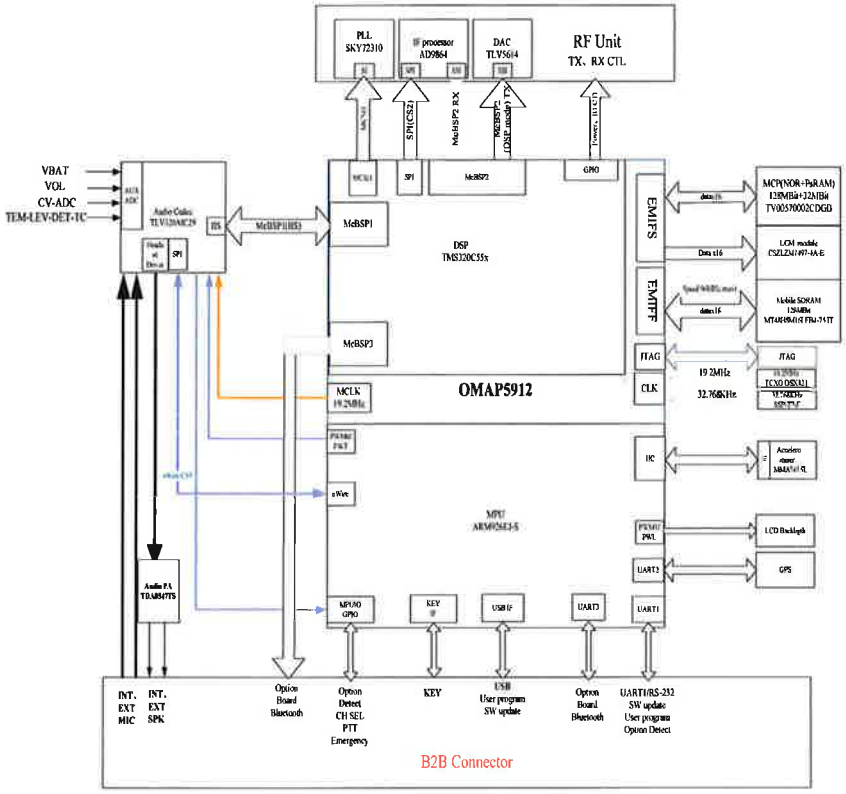


Figure 9 Diagram of Overall Scheme

2.2.2 External Memory

OMAP5912 provides two types of external memory interfaces: external memory interface slow (EMIFS) and external memory interface fast (EMIFF).

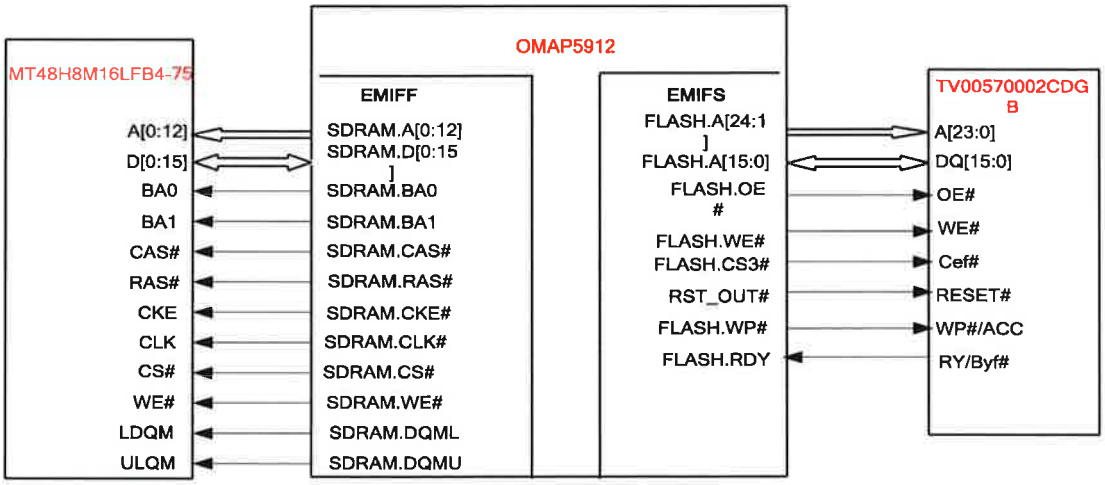


Figure 10 Diagram of External Memory

1) EMIFS

EMIFS is a 16-bit interface, and provides chip-selects CS0~CS3 (CS1 and CS2 can be divided into two 32MB chip-selects), each of which is 64MB. This interface supports memories such as NAND Flash,

NOR Flash, SRAM, and asynchronous and synchronous memories with AD mux or NON mux interface. Also, it supports synchronous burst read, asynchronous read, asynchronous page read and asynchronous write.

2) EMIFF

EMIFF is a 16-bit interface, and supports SDRAM (up to 128MB), mobile SDRAM and mobile DDR. The maximum clock signal of the interface is 96MHz. The system can boot from CS0 (internal ROM), or from CS3 (external memory).

2.2.3 Clock

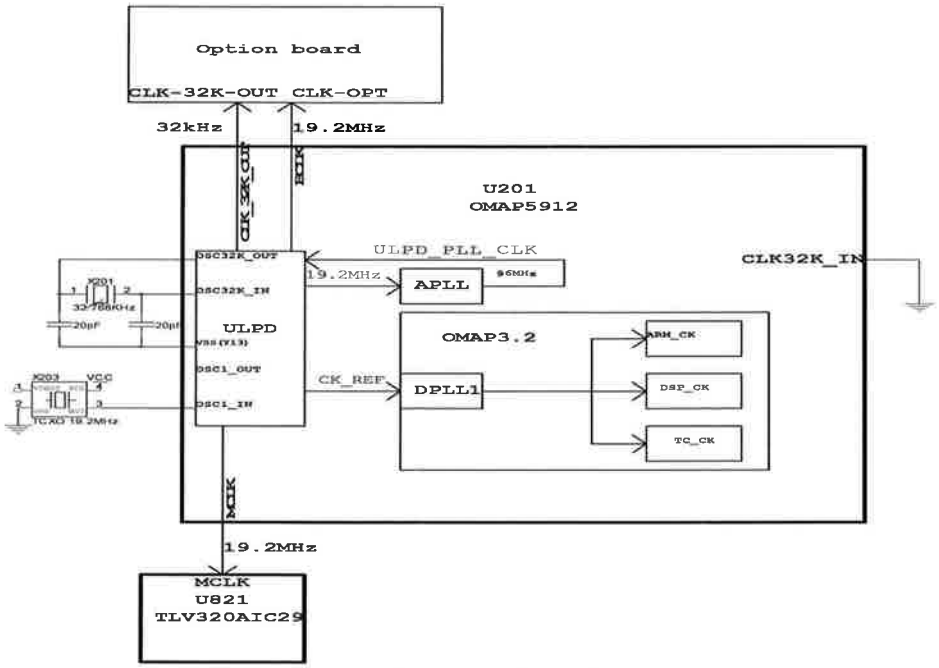


Figure 11 Diagram of Baseband Clock

Input Clock:

(A) 32K Clock: It is also called "sleep clock" and is mainly used for timing and sleeping of the system.

(B) 19.2MHz Clock: It is mainly used to provide input clock for APLL and DPLL.

Output Clock:

Three output clocks are provided: MCLK, BCLK and CLK32K_OUT. MCLK provides 19.2MHz clock to the audio codec; BCLK provides 19.2MHz clock to the option board; and CLK32K_OUT provides 32KHz clock to the option board.

2.2.4 Reset Signal

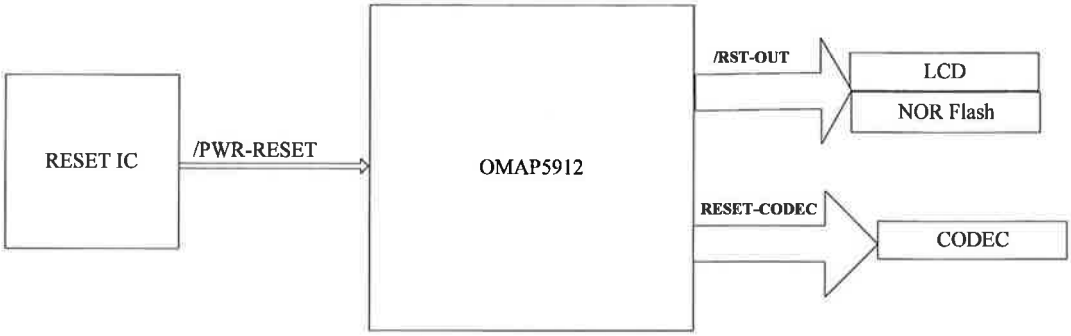


Figure 12 Diagram of Reset Signal

2.2.5 SPI

OMAP5912 has a SPI, which has four chip-selects for connecting four external SPI components. The SPI signals available are SPI.DOUT, SPI.DIN, SPI.CLK and SPI.CS. The system uses SPIF.CS2 to select the IF processor AD9864, to configure register of AD9864. The connection of SPI is shown below.

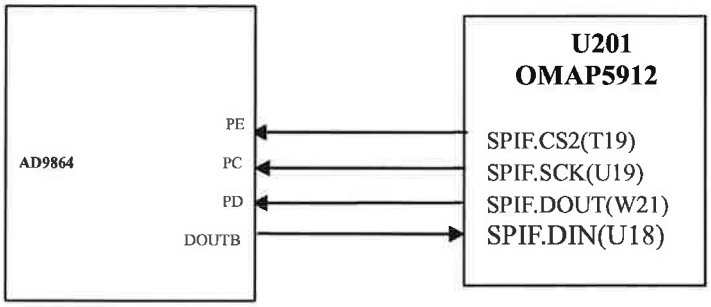


Figure 13 Diagram of SPI Connection

2.2.6 MCBSP

OMAP5912 provides 3 MCBSP interfaces: MCBSP1, MCBSP2 and MCBSP3. MCBSP1 is connected with the I2S interface of the audio codec, to realize two-way transmission of digital voice and data. MCBSP2 uses independent clock and frame synchronization for transmission and reception. AD9864 SSI is connected to the RX end of OMAP5912 MCBSP2. AD9864 works in master mode, while DSP works in slave mode. DAC is connected with the TX end of MCBSP2, and DSP works in master mode. MCBSP3 is connected to the option board. The connection of MCBSP is shown below.

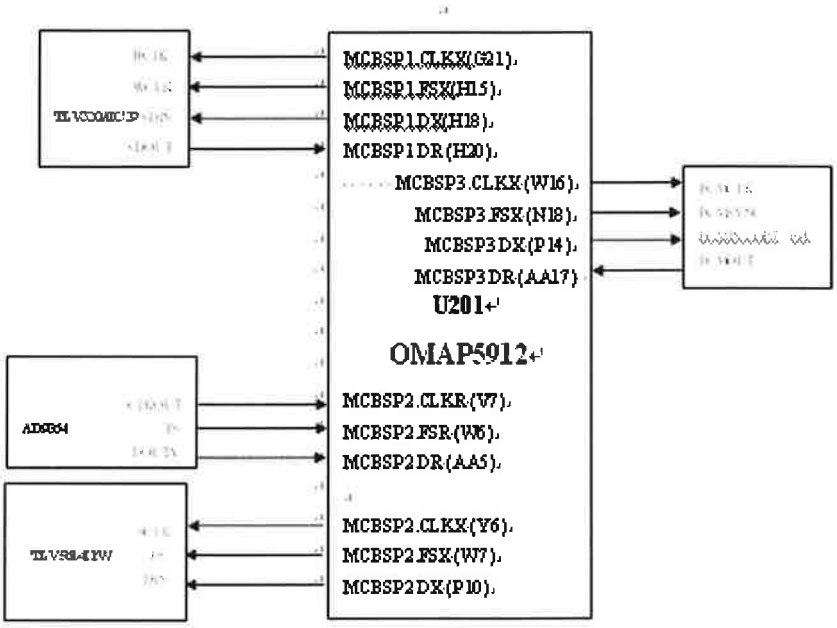


Figure 14 Diagram of MCBSP Connection

2.2.7 USB

OMAP5912 provides 3 USB interfaces, one of which integrates USB transceiver. In this way, the design of USB interface is simplified. The integrated USB transceiver is connected to the accessory jack, and is used for program downloading and data applying.

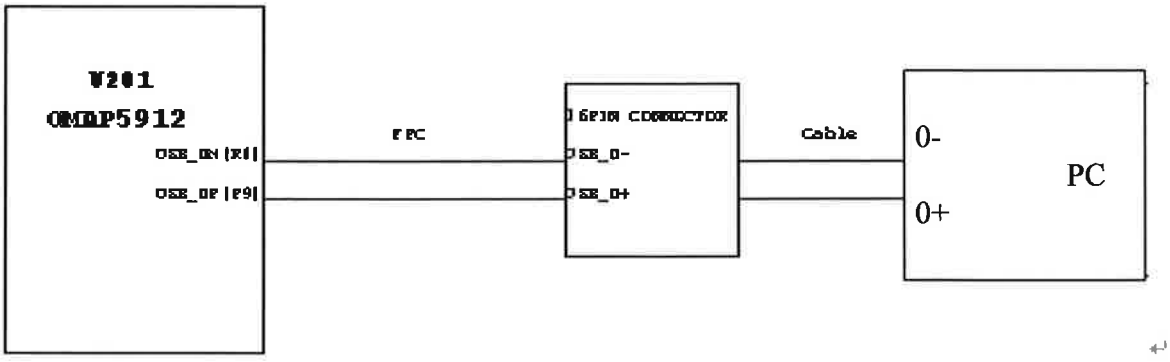


Figure 15 Diagram of USB Interface

2.2.8 UART

OMAP5912 has three UART interfaces (UART1, UART2 and UART3), and supports hardware flow control. The maximum communication rate is 1.5Mbps. The connection of UART is shown below. UART1 is connected with the accessory jack, and is used for updating and programming. UART2 is for GPS, and UART3 is for the option board.

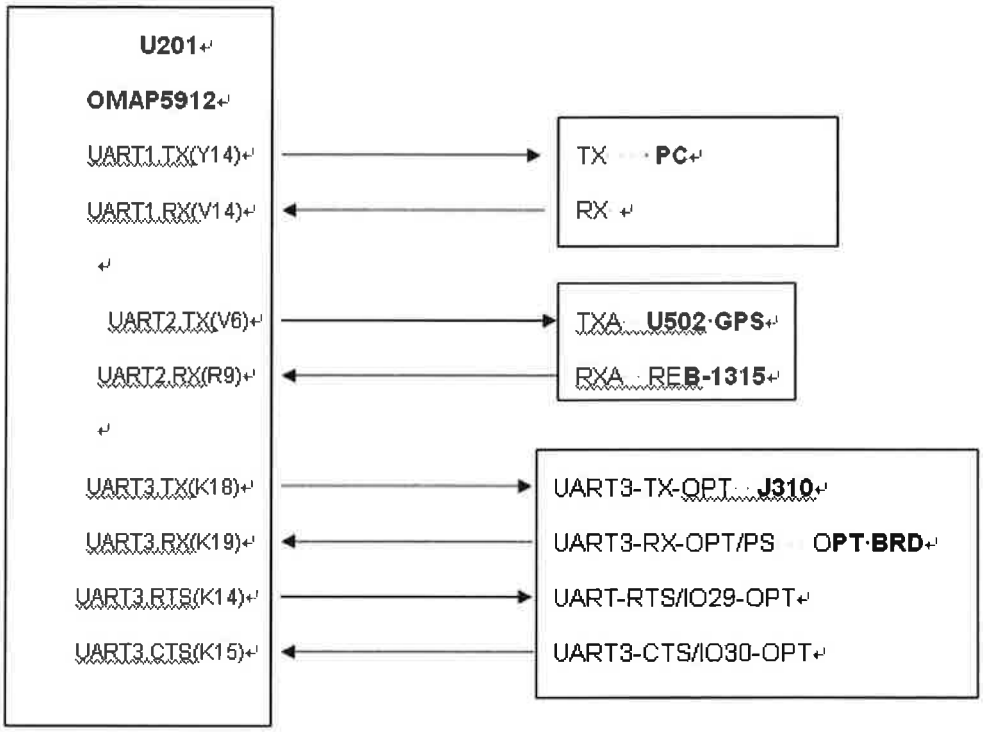


Figure 16 Diagram of UART Interface Connection

2.2.9 I2C

OMAP5912 provides one I2C interface, and supports communication rate of up to 400Kbps. The I2C interface is connected with the acceleration sensor, and works in slave mode. The connection of I2C is shown below.

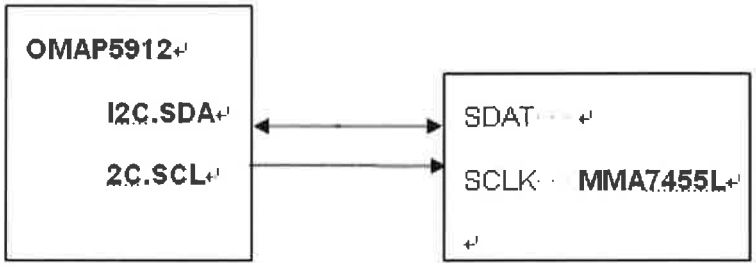


Figure 17 Diagram of I2C Connection

2.2.10 MICROWIRE

OMAP5912 provides a MICROWIRE. The four chip select signals can drive four external components. MICROWIRE is used to configure the audio codec and read the value of its register. It uses the chip select signal 3. The connection is shown below.

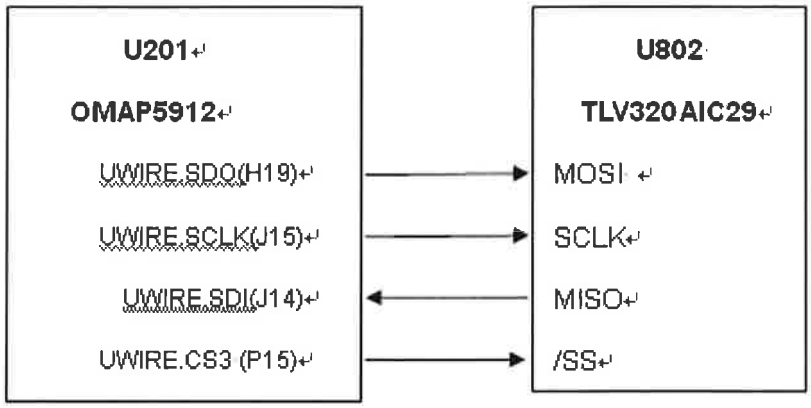


Figure 18 Diagram of MICROWIRE Connection

2.2.11 MCSI1

OMAP5912 has two MCSI interfaces. MCSI1 is used for PLL configuration and data transmission. The connection of MCSI1 is shown below.

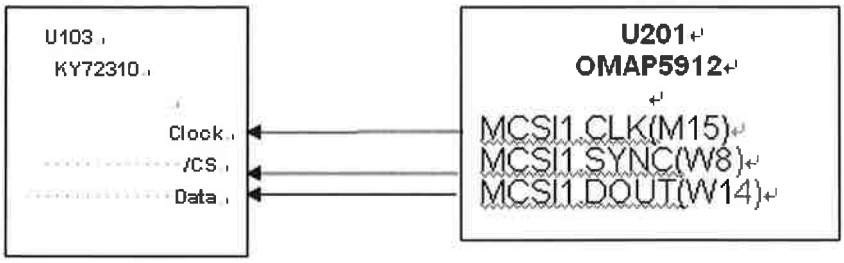


Figure 19 Diagram of SPI Connection

2.3 Audio Section

2.3.1 Audio Diagram

The audio module is mainly for audio input and output. TLV320AIC29 is used as the audio codec to convert and process audio signal and digital signal. The audio amplifier TDA8547TS is used to amplify the analog audio signal. DSP processes digital signal (audio signal encoding/decoding, digital I/Q signal decoding, digital audio signal processing). AD9864 converts and processes the RF IF signal, and sends the undemodulated serial digital I/Q signal to the DSP for processing. Then DAC5614 converts the digital signal output by DSP to analog signal.

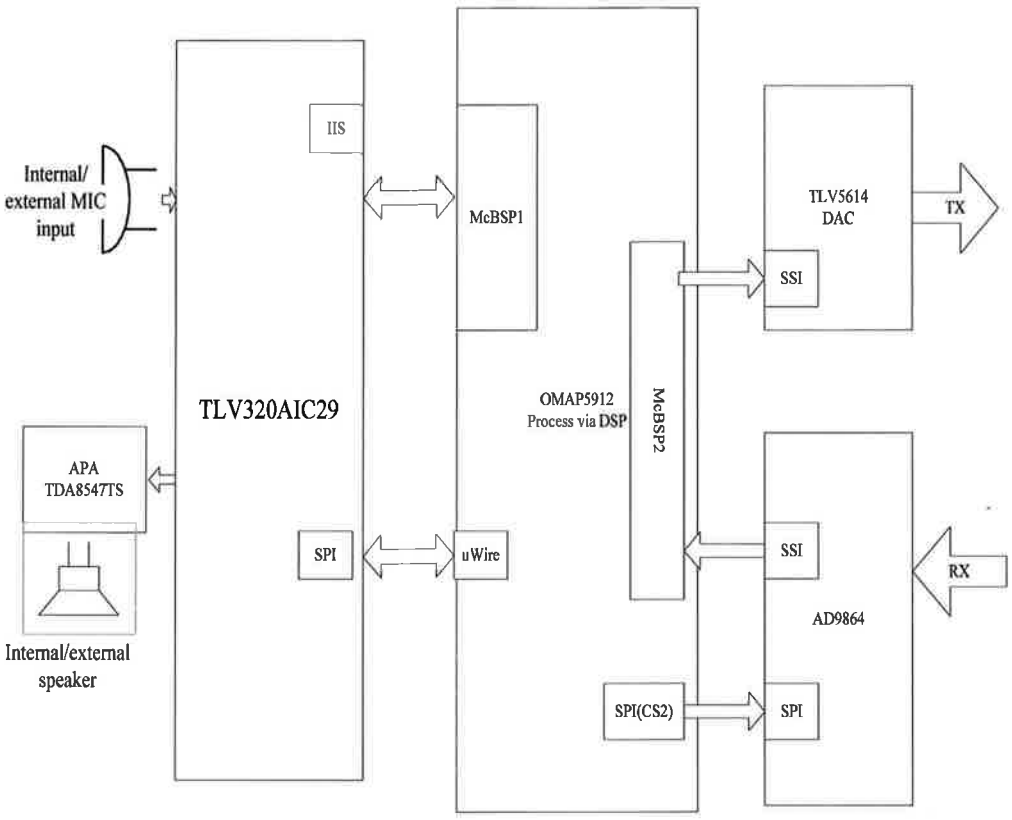


Figure 20 Diagram of Audio Section

2.3.2 Diagram of Signal Flow

The microphone converts the audio signal into electrical signal, which is then amplified by PGA of the codec and sent to ADC of the codec for sampling. After digital audio processing, the signal is output to DSP for processing. Then the signal is sent to DAC (TLV5614), which converts the signal to modulation signal. After modulated and amplified in the RF module, the signal is sent out from the antenna.

The RF signal received by the RF module is converted to digital signal by ADC (AD9864), and is then sent to DSP for demodulation and processing. Then the digital signal is sent to the digital audio processor of the codec for digital audio processing, and is then converted into analog audio signal by DAC of the codec. Finally the signal is amplified by the external audio amplifier (TDA8547TS) to drive the speaker.

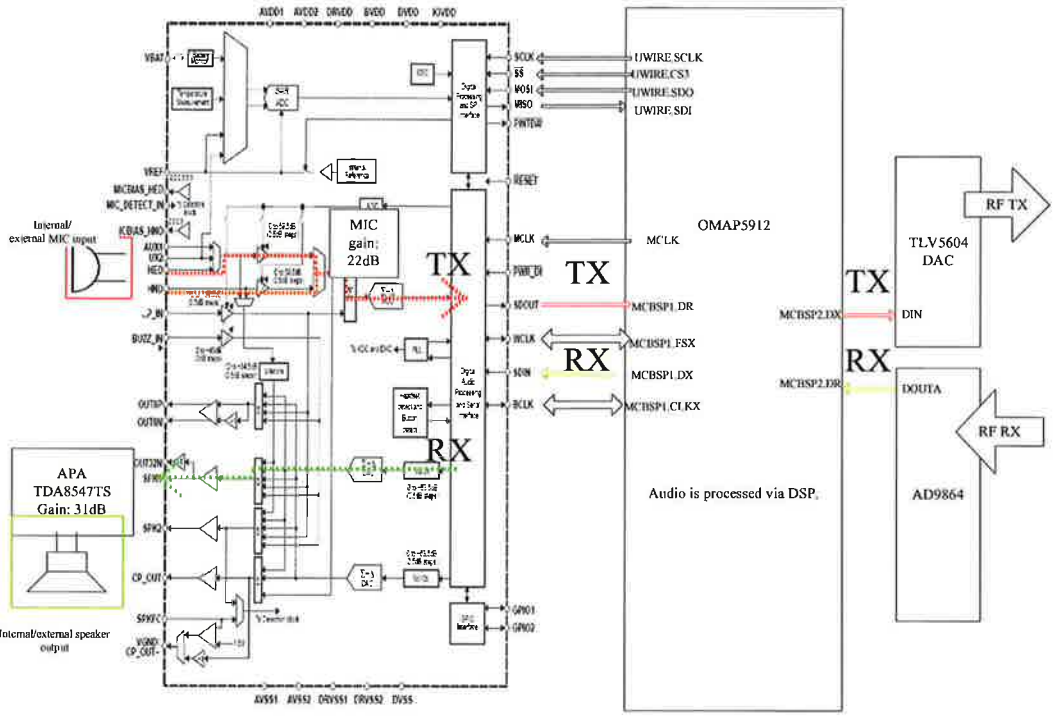


Figure 21 Diagram of Audio Signal Flow

2.3.3 Audio Amplifier

Main parameters of TDA8547TS are listed in the table below:

Rated Power (P_o)	0.5W	R_L =16Ω
Maximum Power (P_{max})	1.2W	R_L =16Ω
Rated Audio Distortion	3%	R_L =16Ω, P_o=0.9W

The operation status of the audio amplifier is controlled via GPIO of OMAP. See the table below.

Mode-Amp	SEL-SPK	MODE	SELECT	OUT
1	1	0	0	OUT2
1	0	0	1	OUT1
0	1	1	1	Standby

Tuning Description

For details about radio tuning, please refer to the help file of DMR Tuner Software supplied by Hytera.

Port Definition

Note: The description related to the LCD is applicable to PD78X/ PD78XG/ HD785/ HD785G only, while the description related to GPS is applicable to PD70XG/ PD78XG/ HD705G/ HD785G only.

J1601: 50-Pin Interface

Pin No.	Name	Function	Valid Level
2, 5, 49	GND	Power supply: ground (analog)	
1 3	AF-CODEC-TO-50PIN AF-50PIN-TO-CODEC	Analog audio signal output/input	
4 6	EXT-MIC+ EXT-MIC-	External MIC interface	
8 10 12 14 16	IO5-OPT IO4-OPT IO3-OPT IO2-OPT IO1-OPT	GPIO pin of the option board	L/H
7	3V6D	Power supply: 3.6V	
9 11	USB-D+ USB-D-	USB data cable	
13	EMERGENCY	Emergency key	L
32 43	DGND	Power supply: ground (digital)	
18	GPIO	GPIO	
20	LED-K-KEY	LED indication for key operation	L
15 17 19 21	KB-R1 KB-R2 KB-R3 KB-R4	Keyboard row	L
22 24 26 28 30	KB-C4 KB-C3 KB-C2 KB-C1 KB-C0	Keyboard column	
23	EXT-PTT	External PTT detection	L
25 27 29	SEL1-Accessory SEL2-Accessory SEL3-Accessory	Accessory identifier	L
34 36	UART1-RX-OPT/PS UART1-TX-OPT/PS	UART1	
38 40 42	UART3-TX-OPT UART3-RX-OPT UART3-CTS/IO30-OPT	UART3	

44	UART3-RTS/IO29-OPT		
31 33 35 37	MCBSP3-FSX-OPT MCBSP3-DX-OPT MCBSP3-WCLK-OPT MCBSP3-DR-OPT	MCBSP3	
39	IIC-SCL-Acce	IIC	
41	IIC-SDA-Acce		
46	EXT-BAT+	Power supply for accessory or option board	
48 50	IN-SPK- IN-SPK+	Internal speaker	
45 47	EXT-SPK- EXT-SPK+	External speaker	

J311: 30-Pin LCD Interface

Pin No.	Name	Function	Valid Level
1 26		Ground (digital)	
2-17	M-D0----M-D15	LCD data	
18	/CS-LCD	LCD chip select	L
19	/RST-OUT	Reset signal	
20	M-A1	Data and command	
21	/WE	Write signal	L
22	/OE	Read signal	L
23	IMO	16/8-bit LCD data selection	
24	3V3D	Power supply: 3.3V	
25	VFLASH	Power supply for IO	
27	3V6D	Power supply for backlight	
28 29 30		Backlight control	L

J2: 20-Pin Option Board Interface

Pin No.	Name	Function	Valid Level
1 3 5 7 9	IO1-OPT IO2-OPT IO3-OPT IO4-OPT IO5-OPT	GPIO	L/H
11 13 15 17	UART3-TX-OPT UART3-RX-OPT UART3-CTS/IO30-OPT UART3-CTS/IO30-OPT	UART3	
2	IIC-SDA-Acce	IIC data	

4	IIC-SCL-Acce	IIC clock	
6 8 10 12	MCBSP3-DR-OPT MCBSP3-WCLK-OPT MCBSP3-DX-OPT MCBSP3-FSX-OPT	MCBSP3	
14		Ground (analog)	
16	AF-50PIN-TO-CODEC	Analog audio signal	
18	AF-CODEC-TO-50PIN	Analog audio signal	
19		Ground (digital)	
20	3V6D	Power supply for digital circuit	

16-Pin Accessory Interface

Pin No.	Name	Function	Valid Level
1	GND	Ground (analog & digital)	
2	SPK-	External speaker-	
3	SEL1-Accessory	Accessory identifier 1	L
4	SEL2-Accessory	Accessory identifier 2	L
5	Emergency	Emergency	L
6	SPK+	External speaker+	
7	USB+ / RTS	USB+ / RTS	
8	USB- / CTS	USB- / CTS	
9	SWB+	Power supply for the accessory interface	
10	MIC-	External MIC-	
11	GPIO	GPIO	
12	MIC+	External MIC+	
13	SEL3-Accessory	Accessory identifier 3 or 1-wire communication interface	L
14	TX	TX end of serial port communication	
15	RX	RX end of serial port communication	
16	PTT	TX control	L

Definition of Accessory Identifiers

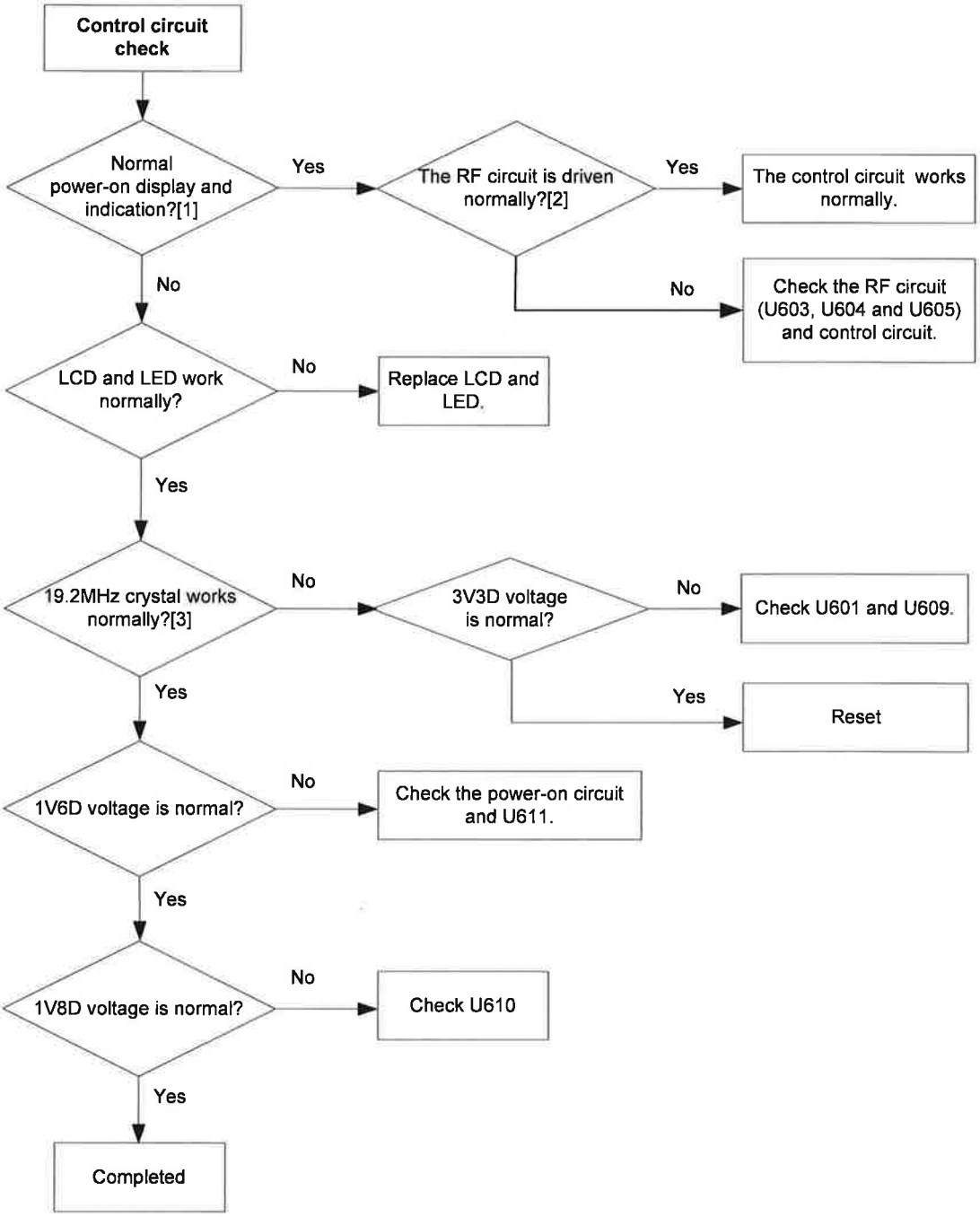
No.	OPT_SEL1	OPT_SEL2	OPT_SEL3	Definition
1	0	0	0	Reserved
2	0	0	1	Reserved
3	0	1	0	USB master mode for the radio
4	0	1	1	For connecting earpieces
5	1	0	0	For connecting MODEM
6	1	0	1	For connecting remote speaker microphones

7	1	1	0	Programming cable (serial port)/ USB slave mode for the radio
8	1	1	1	No accessory

Troubleshooting Flow Chart

Note: The description related to the LCD is applicable to PD78X/ PD78XG/ HD785/ HD785G only, while the description related to GPS is applicable to PD70XG/ PD78XG/ HD705G/ HD785G only.

Control Circuit



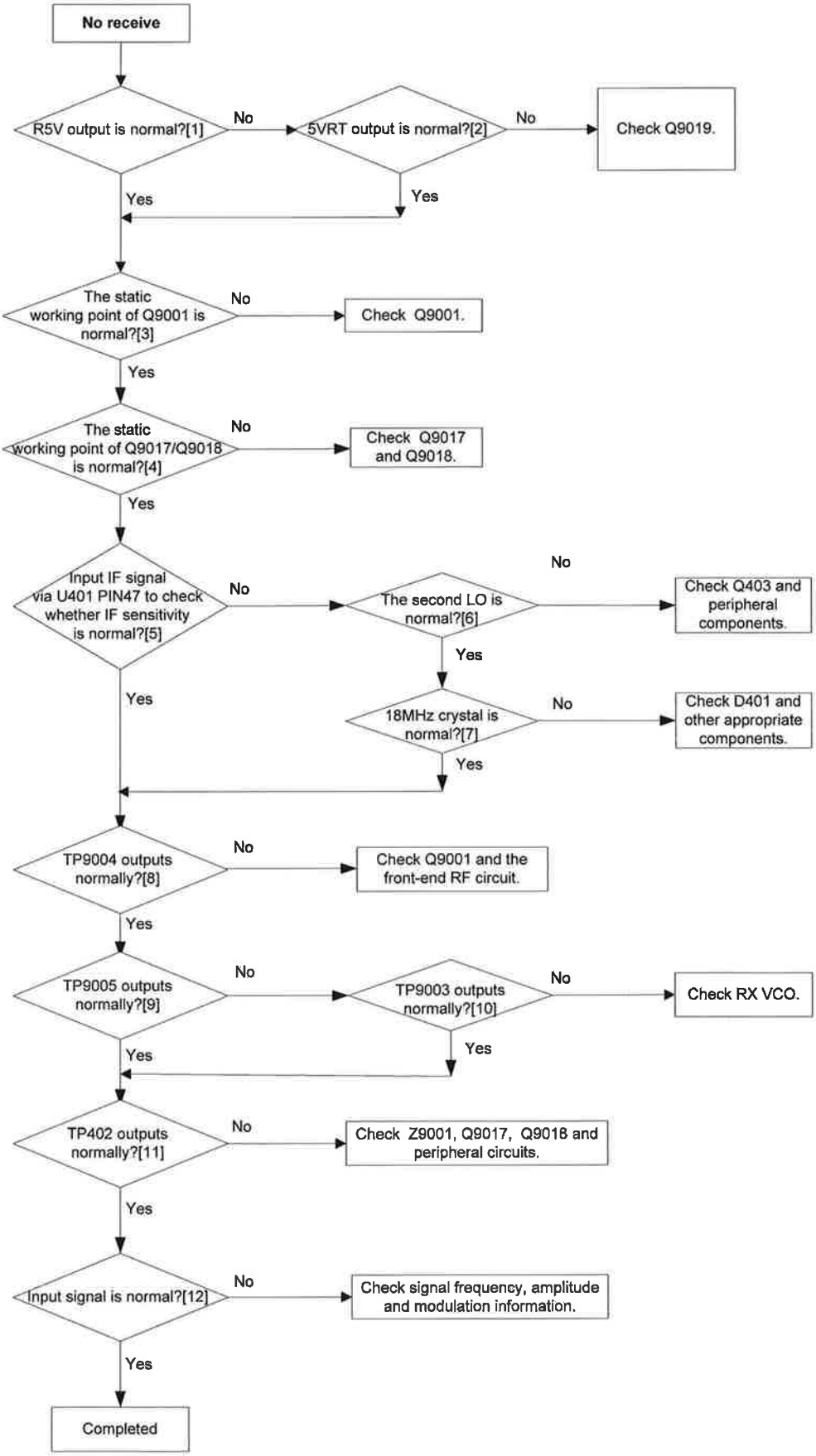
Description of Normal Situation:

[1] The radio shows normal power-on screen, and the backlight is normal.

[2] The RF power supply outputs normally, and the RX channel is on.

[3] Vpp: 700mV~800mV, F: 19.2MHz.

RX Circuit


No receive
R5V output is normal?[1]
No
5VRT output is normal?[2]
No
Check Q9019.
Yes
Yes
The static working point of Q9001 is normal?[3]
No
Check Q9001.
Yes
The static working point of Q9017/Q9018 is normal?[4]
No
Check Q9017 and Q9018.
Yes
Input IF signal via U401 PIN47 to check whether IF sensitivity is normal?[5]
No
The second LO is normal?[6]
No
Check Q403 and peripheral components.
Yes
Yes
18MHz crystal is normal?[7]
No
Check D401 and other appropriate components.
Yes
TP9004 outputs normally?[8]
No
Check Q9001 and the front-end RF circuit.
Yes
TP9005 outputs normally?[9]
No
TP9003 outputs normally?[10]
No
Check RX VCO.
Yes
Yes
TP402 outputs normally?[11]
No
Check Z9001, Q9017, Q9018 and peripheral circuits.
Yes
Input signal is normal?[12]
No
Check signal frequency, amplitude and modulation information.
Yes
Completed

Description of Normal Situation:

[1] Output voltage by Q9019 PIN3: about 4.95V.

[2] Output voltage by U605 PIN4 or input voltage into Q9019 PIN4: about 5V.

[3] Vbe: about 0.74V; Vce: about 2.5V (in the case of no signal reception).

[4] For Q9018, Vbe: about 0.76V; Vce: about 0.95V;
for Q9017, Vbe: about 0.7V; Vce:0.85V (in the case of no signal reception).

[5] Cut off the front-end circuit, and input a 73.35MHz IF signal at TP402 to test IF sensitivity.
Normally, the IF sensitivity is -109dBm.

[6] Frequency of Q403: 71.1MHz.

[7] Frequency of Q411: 18MHz.

[8] Input -30dBm RF signal and test at TP9004. Normally, gain>10dB, output signal>-20dBm.

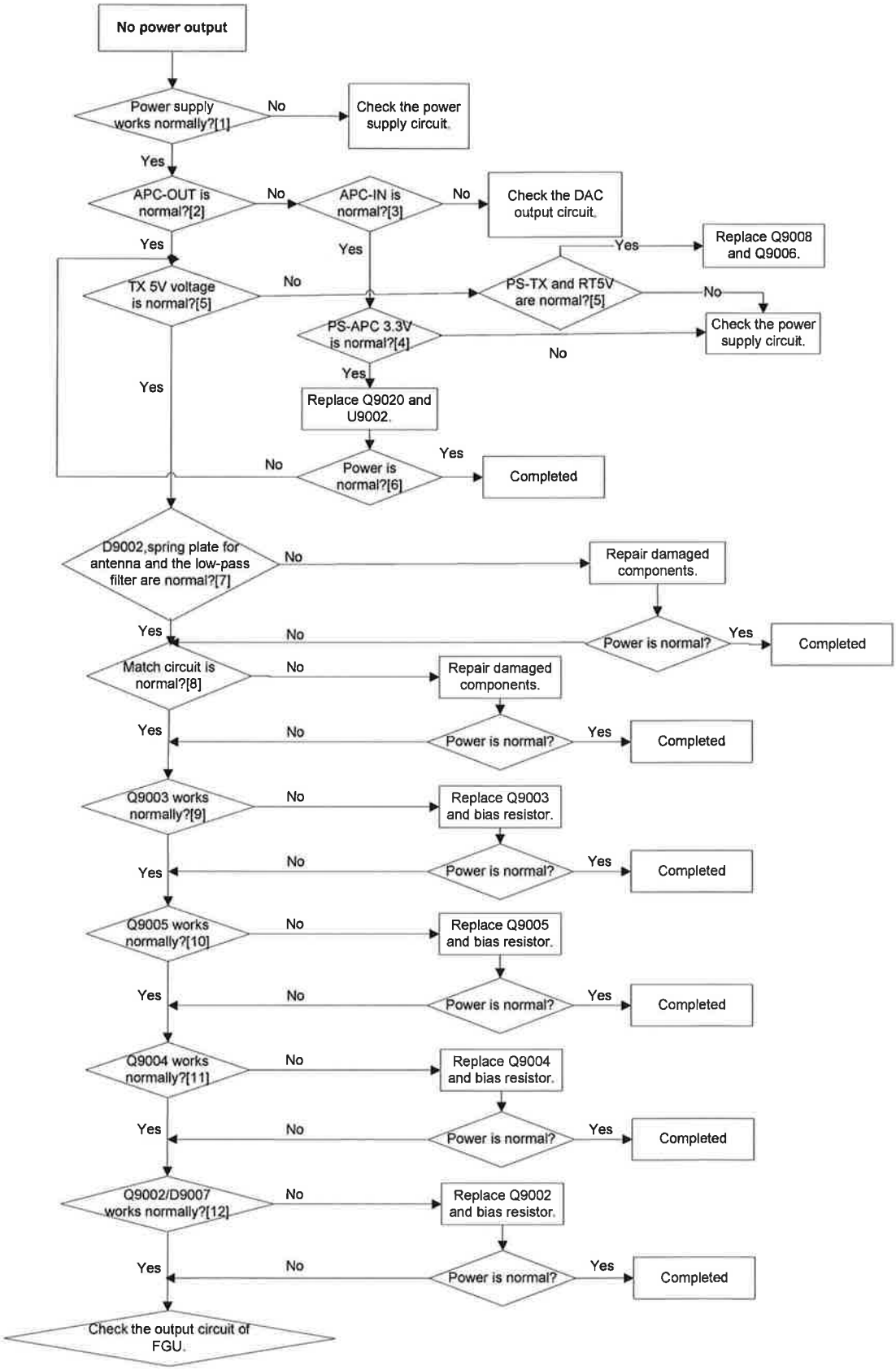
[9] Input -30dBm RF signal and test at TP9005 (do not cut off the rear-end circuit).
Normally, gain>1dB, output signal>-29dBm.

[10] Signal frequency: RF-IF, signal amplitude>2dBm.

[11] For input of -80dBm signal, gain>25dB, output signal>-55dBm;
for input of -30dBm signal, output signal<-20dBm.

[12] The input signal, with standard tuning information (AF=1KHz, FM=3KHz), is -47dBm.

TX Circuit


No power output
Power supply works normally?[1]
No
Check the power supply circuit.
Yes
APC-OUT is normal?[2]
No
APC-IN is normal?[3]
No
Check the DAC output circuit.
Yes
Yes
Yes
Replace Q9008 and Q9006.
TX 5V voltage is normal?[5]
No
PS-TX and RT5V are normal?[5]
No
PS-APC 3.3V is normal?[4]
Check the power supply circuit.
No
Yes
Yes
Replace Q9020 and U9002.
No
Power is normal?[6]
Yes
Completed
D9002,spring plate for antenna and the low-pass filter are normal?[7]
No
Repair damaged components.
Yes
No
Power is normal?
Yes
Completed
Match circuit is normal?[8]
No
Repair damaged components.
Yes
No
Power is normal?
Yes
Completed
Q9003 works normally?[9]
No
Replace Q9003 and bias resistor.
Yes
No
Power is normal?
Yes
Completed
Q9005 works normally?[10]
No
Replace Q9005 and bias resistor.
Yes
No
Power is normal?
Yes
Completed
Q9004 works normally?[11]
No
Replace Q9004 and bias resistor.
Yes
No
Power is normal?
Yes
Completed
Q9002/D9007 works normally?[12]
No
Replace Q9002 and bias resistor.
Yes
No
Power is normal?
Yes
Completed
Check the output circuit of FGU.

Description of Normal Situation:

[1] Voltage of the power supply: about 7.4V.

[2] For low power, APC-OUT: 1.8-2.1V; for high power, APC-OUT: 2.4-2.8V.

[3] For low power, APC-IN: 1-1.3V; for high power, APC-IN: 1.8-2.1V.

[4] PS-APC: about 3.3V.

[5] TX5V: about 5V; RT5V: about 5V; PS-TX: about 3.3V.

[6] High power: about 4.2W; low power: about 1.2W.

[7] Start-up voltage of D9002: about 0.7V. The low-pass filter must be soldered appropriately and remain in good condition. The spring plate for the antenna must be well fitted into the antenna connector.

[8] The match components must not be soldered inappropriately or damaged.

[9] Vdd: about 7.3V; for low power, Vgg: 1-1.2V; for high power, Vgg: 1.35-1.55V.

[10] Vdd: about 7.3V; for low power, Vgg: 1.8-2.1V; for high power, Vgg: 2.4-2.8V.

[11] Vc: about 4.8V; Vb: about 1.4V; Ve: about 1.1V.

[12] Vc: about 4.7V; Vb: about 0.7V; Ve: 0V. Start-up voltage of D9007: about 0.7V.

Note: The above check operations should be made under 7.4V voltage.

FGU


FGU check
5VFGU, 3V3ARF, 3V3DRF are normal?
No
Check the power supply circuit.
Yes
VCO oscillates?
No
Q106 and Q107 are normal?[1]
Yes
Q104 and Q108 are normal?[2]
No
Replace Q104 and Q108.
No
Replace Q106 and Q107.
Yes
Check Q104, Q108 and peripheral components.
Yes
CV voltage is normal?[3]
No
L110 and L116 are normal?[4]
No
Replace L110 and L116.
Yes
Yes
Replace Q101 and Q102.
No
Q101 and Q102 are normal?[5]
Yes
Check Q101, Q102 and peripheral components.
Feedback is output?
No
Check the feedback circuit.
Yes
19.2MHz crystal oscillates?
No
Check the 19.2MHz circuit.
Yes
Sky72310 clock is normal?[6]
Yes
Completed
No
Check the data circuit of the control circuit.

Description of Normal Situation:

[1] During transmission, output voltage by Q107 PIN3: about 4V.
During reception, output voltage by Q106 PIN3: about 4V.

[2] During transmission, voltage at Q108 E: about 1.8V.
During reception, voltage at Q104 E: about 1.8V.

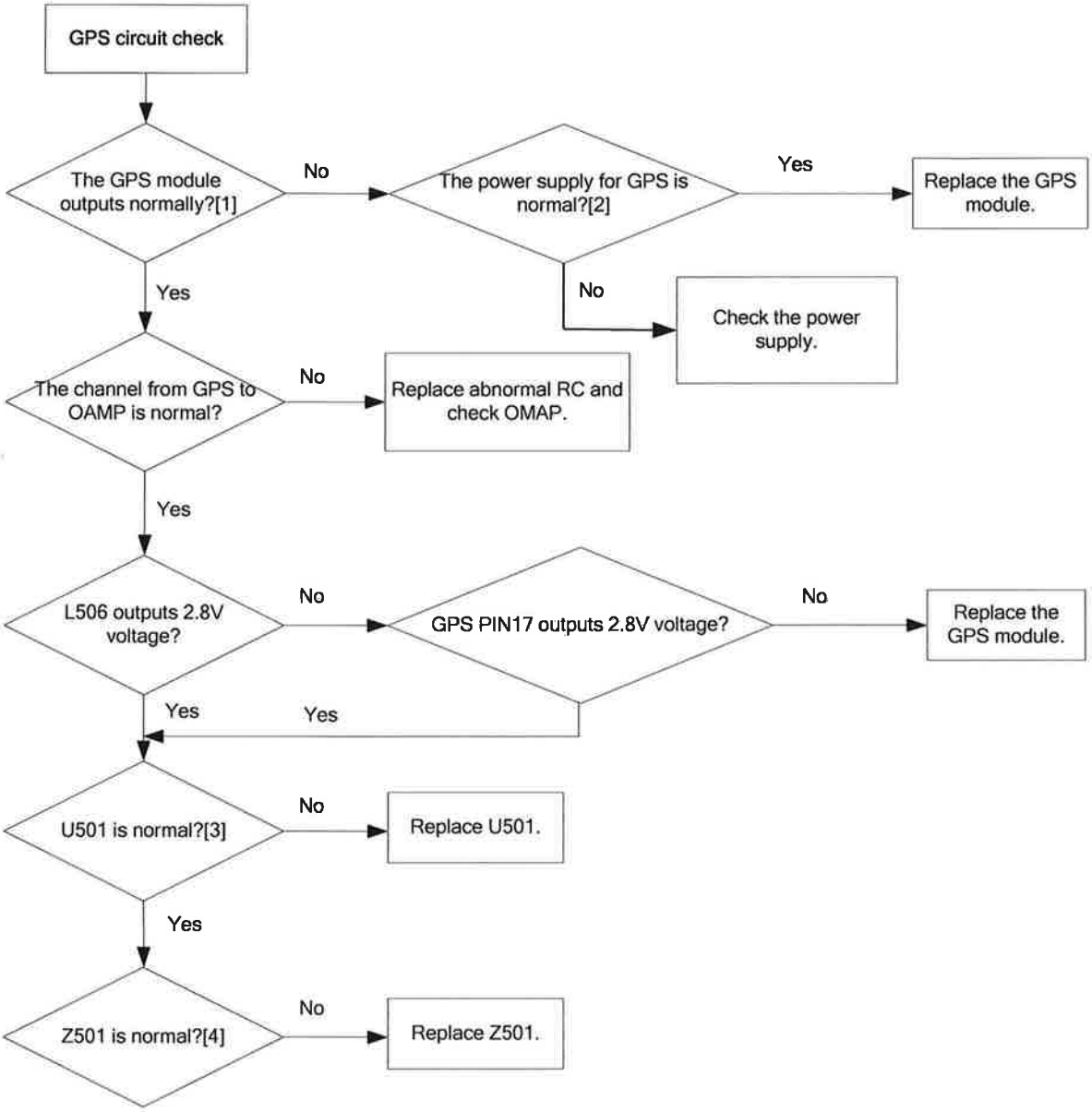
[3] The CV value varies with frequencies. Generally, it is within the range 0.5V-4.5V.

[4] L110/L116 is on.

[5] Voltage at Q101/Q102 B: about 0.7V.

[6] MCSI-CLK-PLL outputs 960KHz clock.

GPS Circuit



Description of Normal Situation:

[1] Detect with a multimeter. The voltage of TP502 changes within the range 1.2V~2.8V.

[2] Voltage at L502 and L505: about 3.3V.

[3] Gain for U501 (@1.57542GHz):> 15dB.

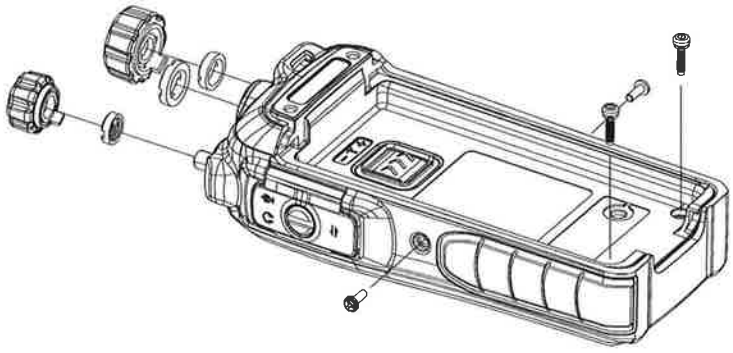
[4] Insertion loss for Z501 (@1.57542GH): < 4dB.

Disassembly and Assembly

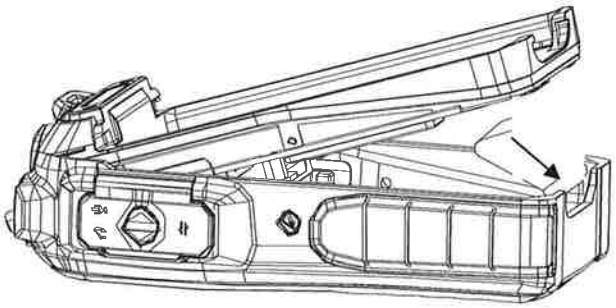
Note: The disassembly and assembly operations for PD70X/ PD70XG/ HD705/ HD705G and PD78X/ PD78XG/ HD785/ HD785G are similar. This section illustrates based on PD78X/ PD78XG/ HD785/ HD785G.

Disassembling the Chassis

1. Turn off the radio, and remove the two screws on the sides of the radio.
2. Remove the two screws on the bottom of the chassis.
3. Remove the Radio On-Off/Volume Control knob and Channel Selector knob.



4. Push the chassis upwards, and take the 50-pin connector down (see the arrow in the figure below). Then you can take the chassis out.

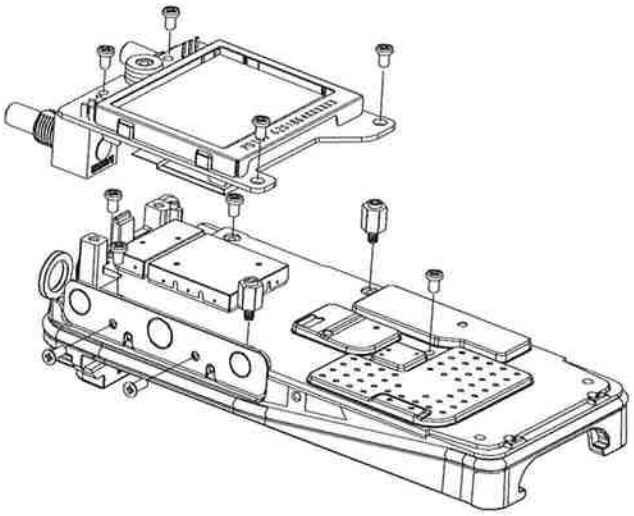


Disassembling the TX and RX Units

1. Remove the screws on the PTT board.
2. Remove the screws on the LCD board.

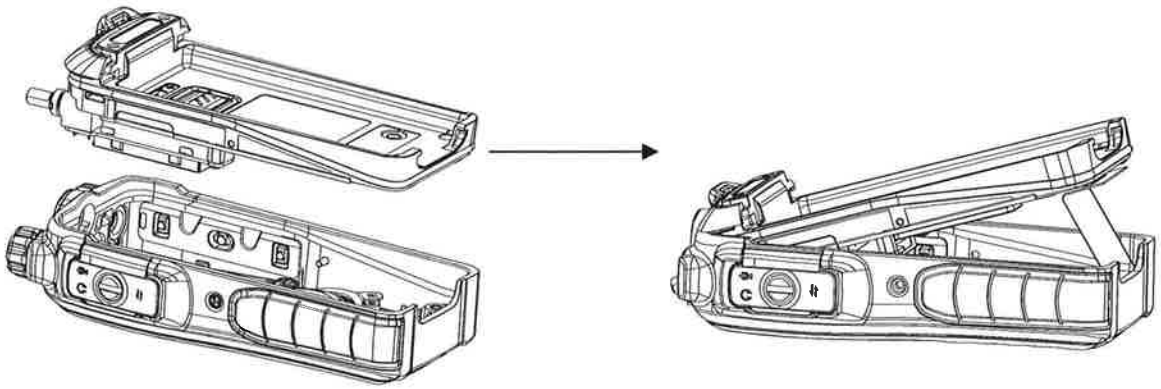
Note: For PD70X/ PD70XG/ HD705/ HD705G, please remove the screws on the small board.

3. Remove the screws on the main board.
4. Take the main board down the chassis.



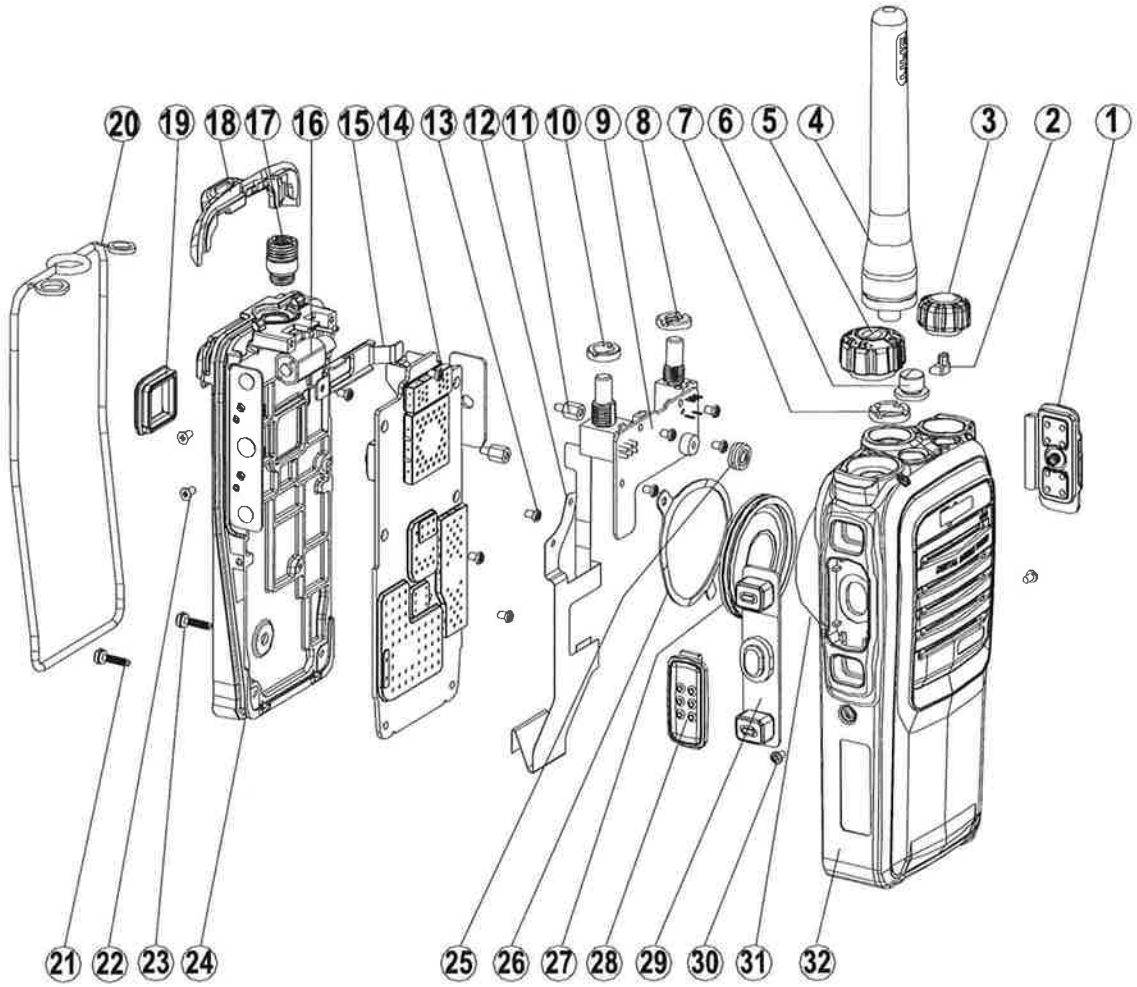
Precautions for Assembly

1. Make sure the waterproof ring surrounding the chassis is well fitted into the slot.
2. Insert the chassis into the radio case.
3. Attach the 50-pin board-to-board connector.
4. Press the bottom of the chassis downwards to fit the chassis into the radio case.

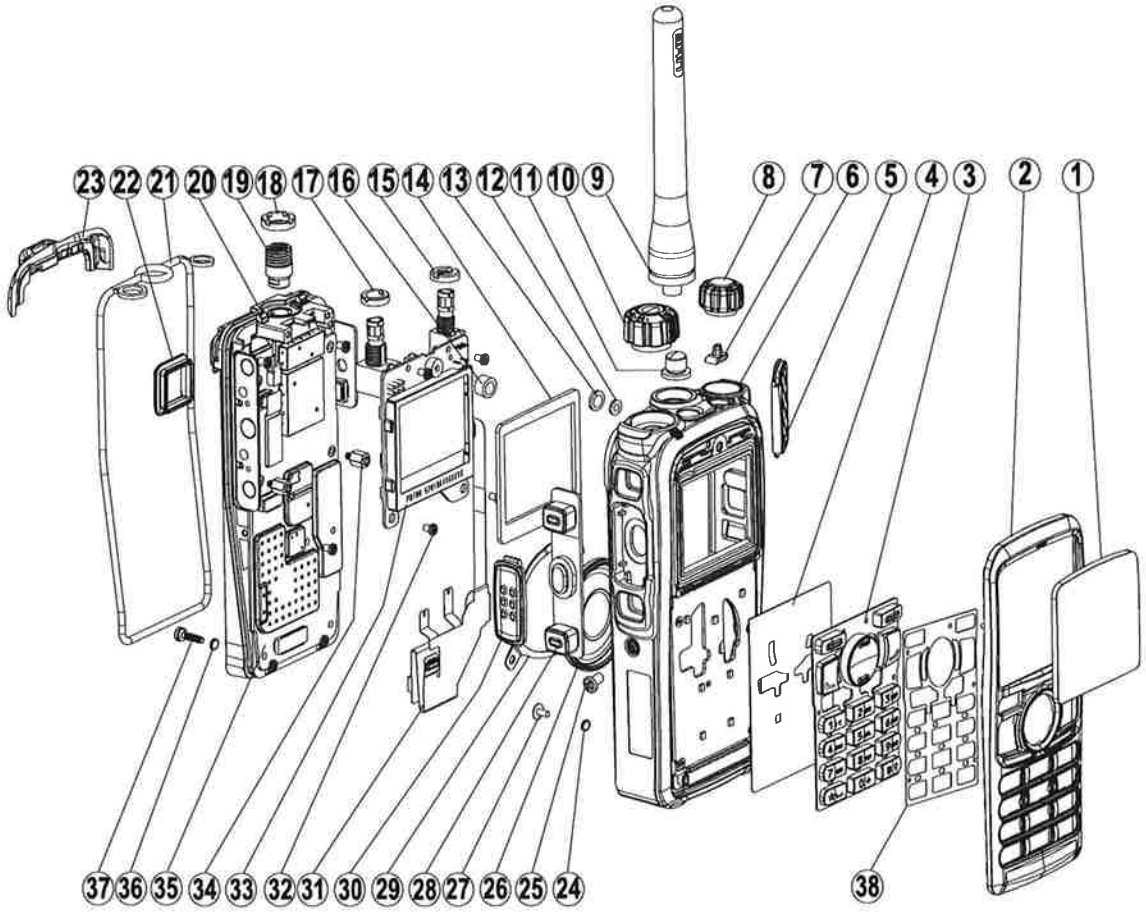


Exploded View

PD70X/ PD70XG/ HD705/ HD705G

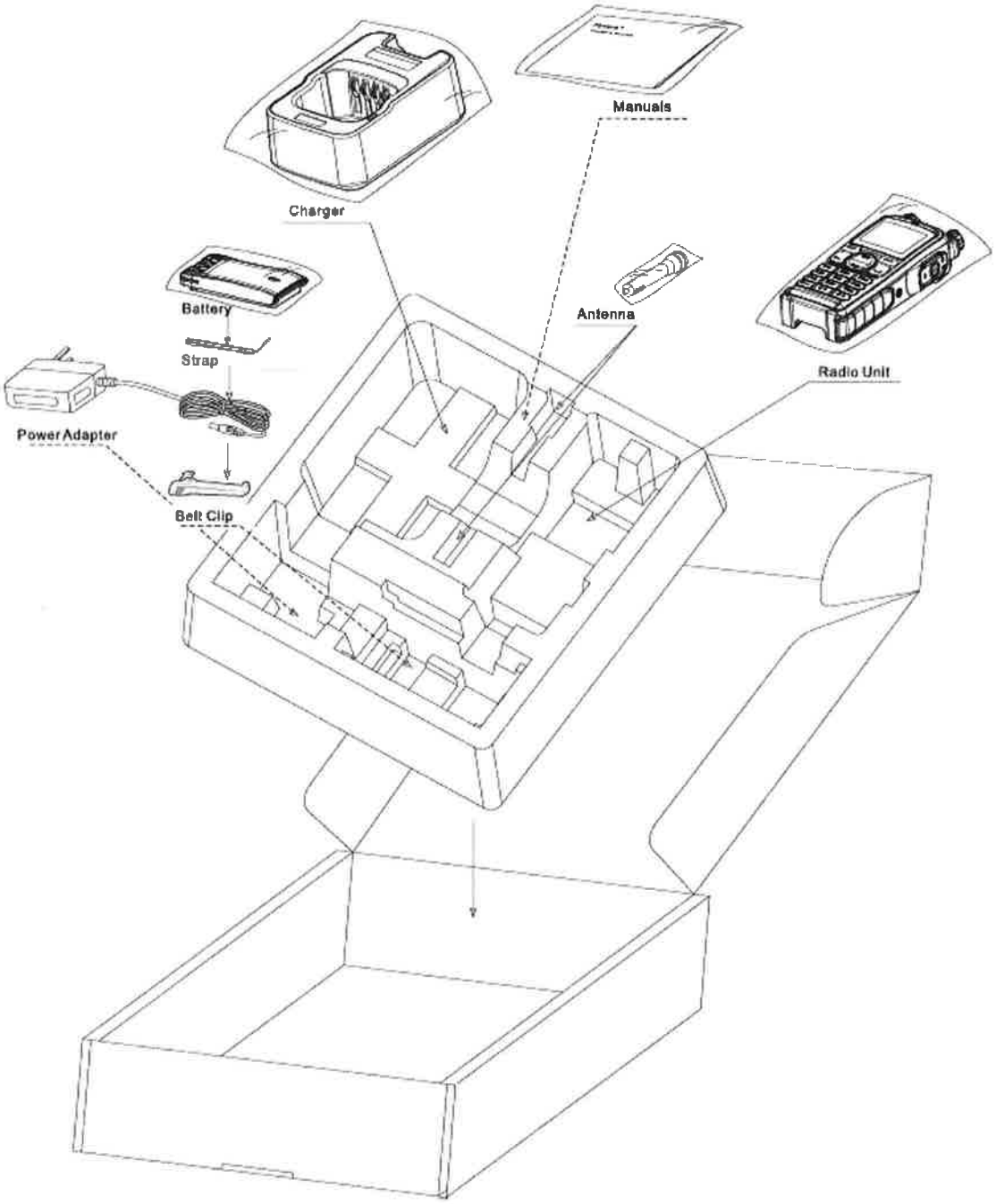


PD78X/ PD78XG/ HD785/ HD785G



Packing Guide

Note: This section takes PD78X/ PD78XG/ HD785/ HD785G for example.



Specifications

General		
Frequency Range		400-470MHz
Channel Capacity		PD70X/ PD70XG/ HD705/ HD705G: 32 PD78X/ PD78XG/ HD785/ HD785G: 1024
Channel Spacing		25/20/12.5KHz
Operating Voltage		7.4V (rated)
Battery		2000mAh Li-Ion battery
Battery Life (5-5-90 Duty Cycle, High TX Power) High-capacity 2000mAh Li-Ion Battery		Analog: Above 10.5 Hours Digital: Above 14 Hours
Operating Temperature		-30℃ ~ +60℃
Dimensions (H×W×D) (with standard battery, without antenna)		PD70X/ PD70XG/ HD705/ HD705G: 125×55×35 mm /4.921×2.165×1.378 inch PD78X/ PD78XG/ HD785/ HD785G: 125×55×37 mm /4.921×2.165×1.458 inch
Weight (with antenna & standard battery)		PD70X/ PD70XG/ HD705/ HD705G: 335g /0.74lb PD78X/ PD78XG/ HD785/ HD785G: 355g /0.78lb
Frequency Stability		±1.5ppm
Receiver		
Sensitivity	Analog	0.3μV (12dB SINAD) 0.22μV (Typical) (12dB SINAD) 0.4μV (20dB SINAD)
	Digital	0.3μV /BER5%
Adjacent Channel Selectivity TIA-603 ETSI		60dB @ 12.5 kHz / 70dB @ 20&25 kHz 60dB @ 12.5 kHz / 70dB @ 20&25 kHz
Intermodulation TIA-603 ETSI		70dB @ 12.5/20/25 kHz 65dB @ 12.5/20/25 kHz
Spurious Response Rejection TIA-603 ETSI		70dB @ 12.5/20/25 kHz 70dB @ 12.5/20/25 kHz
Rated Audio Power Output		0.5W (16Ω load)
Rated Audio Distortion		≤3%

Transmitter	
RF Power Output	4W/1W
Conducted/Radiated Emission	-36dBm<1GHz -30dBm>1GHz
Modulation Limiting	±2.5kHz @ 12.5 kHz ±4.0kHz @ 20 kHz ±5.0kHz @ 25 kHz
FM Noise	40dB @ 12.5 kHz 43dB @ 20KHz 45dB @ 25 kHz
Audio Distortion	≤3%
GPS	
TTFF (Time To First Fix) Cold Start	<1 minute
TTFF (Time To First Fix) Hot Start	<10 seconds
Horizontal Accuracy	<10 meters

All Specifications are tested according to applicable standards, and subject to change without notice due to continuous development.

Appendix

Table of Blind Spots

No.	Blind Spot (MHz)
1	403.2
2	422.4
3	441.6
4	460.8
5	414
6	432
7	450
8	468
9	434.7
10	407.4625
11	407.475
12	411.725
13	411.7375
14	416
15	424.5375
16	426.6625
17	428.8
18	430.9375
19	435.2
20	439.4625
21	439.475
22	443.7375
23	448
24	452.2625
25	452.275
26	456.525

27	456.5375
28	458.6625
29	465.0625
30	465.075